DETAILED DESCRIPTION OF THE PRESENT INVENTION

Hereinafter, embodiments of the present invention will be described in detail with reference to the attached drawings. However, the embodiments of the present invention can be modified into various other forms, and the scope of the present invention must not be interpreted as being restricted to the embodiments. The embodiments are provided to more completely explain the present invention to those skilled in the art., like reference numerals in the drawings denote the same members.

Referring to FIG.2, the FFT apparatus for compensating for OFDM output bit signal according to the present invention includes a scale detection unit 39, a scale count unit 41 and a compensation unit 43.

The FFT apparatus according to the present invention preferably has a bus 30 as a data pathway, an input buffer unit 33 located at the input end for storing the input signal and a butterfly operation unit 37 for performing a butterfly operation.

The scale detection unit 39 calculates and outputs a scale factor for controlling the bit value of the input signal from the butterfly operation unit 37 within the predetermined bit limit of the OFDM signal input to the input buffer unit 33.

The scale count unit 41 cumulatively counts a count figure corresponding to the scale factor that is input from the scale detection unit 39, and then outputs the result.

The compensation unit 43 controls the bit value of the signal that is input from the butterfly operation unit 37 according to both of the values from the scale detection unit 39 and scale count unit 41, and then outputs the result.

It is preferable to insert a first operation unit 35 in between the input buffer unit 33 and the butterfly operation unit 37. The first operation unit 35 divides the bit value of the later input signal by the scale factor of the first input signal, thereby performing the butterfly operation in a manner of considering the scale factor from the scale detection unit 39. It is also preferable to insert an output buffer unit 45 to the output end to store the output signal from the butterfly operation unit 37 at each stage. Also, the control unit 31, which controls signal flow, can be connected to feed the signal stored in the output buffer unit 45 back to the input buffer unit 33 until the number of butterfly operations reach the predetermined number of stages **n**. The signal calculated at the final stage of the predetermined number of stages **n** through the butterfly operation, is outputted to the compensation unit 43.

The preferred embodiment of the FFT apparatus for compensating an OFDM output bit signal will be described below in detail.

According to the preferred embodiment of the present invention, the butterfly operation is performed utilizing a radix-2 algorithm. A signal is inputted to the input buffer unit 33 by 8 bits (I=8bits) under the control of the control unit 31. A bit limit of the scale detection unit 39 is set to 12 bits.

FIG. 3 is a flowchart showing the steps of calculating the scale factor **Sf** of the scale detection unit 39. First, the bit value **Vo** of the butterfly-

operated signal outputted from the butterfly operation unit 37 and the bit value **I** of the signal input to the input buffer unit 33 are received (step S31). Next, it is determined whether the absolute value $|Vo|$ of the bit value **Vo** is greater than **1024** (step S32). If the absolute value $|Vo|$ of the bit value **Vo** is greater than **1024**, the scale factor, which is a division factor used for controlling a signal value within the predetermined bit limit of the OFDM bit signal, is set to **4** (step S33). On the other hand, if the absolute value $|Vo|$ of the bit value **Vo** of the butterfly-operated signal is less than **1024**, then it is determined if the absolute value |Vo| is greater than **512** (step S34). If the absolute value |Vo| is greater than **512** in S34, then the scale factor **Sf** is set to **2** (step S35), while if the absolute value |Vo| is less than **512**, then the scale factor is set to **1** (step S36). The scale factor **Sf**, that is set in this way, is outputted to the first operation unit 35 and the scale factor **Sfn** of the final stage is outputted by the control unit 31 to the first operation unit 35 and to the compensation unit 43, respectively.

FIG. 4 is a detailed block diagram showing the compensation unit 43 of FIG. 2 in detail.

As shown in FIG. 4, the compensation unit 43 includes a second operation unit 55, a division and multiplication selection unit 51, a coefficient calculation unit 53, a division and multiplication calculation unit 57, a bit compensation unit 58 and an adder unit 59.